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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,196	09/09/2003	Kenji Sera	Q77403	1621

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,196	SERA ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) *1-20,38,39,41,44,45,47 and 49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-37,40,42,43,46,48 and 50-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/24/03, 9/9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Election dated 01/28/2005.

Election/Restrictions

1. Claims 1-20, 38-39, 41, 44-45, 47, and 49 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions. Election was made **without** traverse in the reply filed on 01/28/2005.

2. Applicant's election without traverse of claims 21-37, 40, 42-43, 48 and 50-52 in the reply filed on 01/28/2005 is acknowledged.

Oath/Declaration

3. Oath/Declaration filed on 09/09/2003 has been considered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 24, 40, 42-43, 48, 50-62 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

► With respect to claim 24,

line 18, "said switch circuit" lacking antecedent basis should be changed to "said first switch circuit"

lines 28-29, it is not clear which "a second switch circuit for controlling an activation and deactivation of said output amplification stage" is intended to which switch circuit as defined by applicant's specification or figure.

- With respect to claim 29,

line 41, "said differential stage" should be changed to "said first differential stage" to clarify scope of the claim.

line 53, "said differential stage" should be changed to "said second differential stage" to clarify scope of the claim.

- With respect to claim 40,

it is not clear that "the transistor" refers to which transistor of the differential amplifier circuit of claim 21.

- With respect to claims 42-43,

scope of the claims can not be defined. it is not clear that "the transistor" refers to which transistor of the differential amplifier circuit of claim 21.

- With respect to claim 48,

it is not clear "said transistor the differential amplifier circuit" means.

- With respect to claim 50,

the scope of claim can not be defined. It is not clear which two sets of "a plural of transistors" are intended to and/or where these two sets of "a plural of transistors" are located.

- With respect to claims 51-52,

  it is not clear that "the transistors" refers to which transistors of the claim. It is not clear which "the transistors" are intended to and/or where "the transistors" are located.

- With respect to claims 53-54,

  it is not clear "said transistor" refers to which transistor as defined in claim 24.

- With respect to claims 55-56,

  it is not clear "said transistor" refers to which transistor as defined in claim 25.

- With respect to claims 57-58,

  it is not clear "said transistor" refers to which transistor as defined in claim 29.

- With respect to claims 59-60,

  it is not clear "said transistor" refers to which transistor as defined in claim 35.

- With respect to claims 61-62,

  it is not clear "said transistor" refers to which transistor as defined in claim 36.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21-37, 40, 46, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchi [US 6,567,327].

► With respect to claims 21-23 and 40, Tsuchi (fig. 8, cols 1-44) discloses a differential amplifier circuit comprising:

- a differential stage (21) including:

  a differential pair (213, 214) for differentially receiving signal voltage supplied to a input pair thereof;

  a load element pair (211, 212) connected between an output pair of the differential pair (connection between transistor 211 & 212 and connection between transistors 212 and 214) and a first power supply (V_{DD});

  a current source (215) connected between said differential pair and a second power supply (V_{ss}) and supplying a current to said differential pair;

  said differential pair and/or said load element pair being comprised of transistors (211, 212, 213, 214) each having relatively low threshold value; and

  a switch circuit (521) inserted in a current path of said differential stage for controlling an activation and deactivation of said differential stage, said switch circuit inherently including at least one transistor which is controlled to be on and

off by a control signal supplied to a control terminal thereof, said switch circuit (521) connects in series with said power source (215).

Tsuchi et al does not expressly disclose in written disclosure that said at least one transistor of said switch circuit (521) has a threshold value higher than that of the transistor having relatively low threshold value.

However, it would have been obvious for those skilled in the art to have changed the gate to source area of transistors of reference circuit to obtained desired threshold value(s), which can be either high/low depend on the intended use of the invention.

► With respect to claim 24, Tsuchi (fig. 8, cols 1-44) discloses a differential amplifier circuit comprising:

- a differential stage (21) including:

  a differential pair (213,214) for differentially receiving signal voltage supplied to a input pair thereof;

  a load element pair (211, 212) connected between an output pair of the differential pair (connection between transistors 211 & 213 and connection between transistors 212 & 214) and a first power supply (V_{DD}); and

  a current source (215) connected between said differential pair and a second power supply (V_{SS}) and supplying a current to said differential pair; and
- an output amplification stage (32) receiving an output of said differential stage and having an output terminal for outputting an output signal, said output amplification stage including an output stage transistor connected between said output terminal and said first power supply;

- said differential pair and/or said load element pair being comprised of transistors (211, 212, 213, 214) each having relatively low threshold value;
- a first switch circuit (521) for controlling an activation and deactivation of said differential stage, wherein said switch circuit inherently comprises a transistor connected in series with said current source (215) between said differential pair and a second power supply, and including a control terminal for receiving a control signal to be controlled to be on and off, or said first switch circuit is constituted by said current source comprised of a transistor having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving a control signal to be controlled to be on and off;
- a second switch circuit (532) of said output amplification stage (30) for controlling an activation and deactivation of said output amplification stage, including a transistor connected between the control terminal of said output stage transistor and one of said first and second power supplies, and including a control terminal for receiving a control signal to be controlled to be on and off complementarily with the transistor constituting said first switch circuit.

Tsuchi et al does not expressly disclose in written disclosure that transistors of said first and second switch circuit have threshold values higher than that of the transistor having relatively low threshold value.

However, it would have been obvious for those skilled in the art to have changed the gate to source area of transistors of reference circuit to obtained desired threshold value(s), which can be either high/low depend on the intended use of the invention.

► With respect to claim 25, Tsuchi (fig. 8, cols 1-44) discloses a differential amplifier circuit comprising:

- a differential stage including:

  a differential pair (213,214) for differentially receiving signal voltage supplied to a input pair thereof;

  a load element pair (211, 212) connected between an output pair of the differential pair and a first power supply, said load element pair comprised of a transistor pair, conductivity type of which is opposite that of a transistor pair composing said differential pair; and

  a current source (215) connected between said differential pair and a second power supply and supplying a current to said differential pair; and
- an output amplification stage (30) receiving an output of said differential stage and having an output terminal for outputting an output signal, said output amplification stage including an output stage transistor connected between said output terminal and said first power supply;
- said differential pair and/or said load element pair being comprised of transistors (211, 212, 213, 214) each having relatively low threshold value;
- a first switch circuit (521) for controlling an activation and deactivation of said differential stage, wherein said switch circuit inherently comprises a transistor

connected in series with said current source between said differential pair and a second power supply and including a control terminal for receiving a control signal to be controlled to be on and off, or said first switch circuit is constituted by said current source;

- a transistor (311) connected in series with said output stage transistor between said output terminal and said first power supply, and including a control terminal for receiving said control signal to be controlled to be on and off in phase with said transistor constituting said first switch circuit.

Tsuchi et al does not expressly disclose in written disclosure that the transistor of said first switch circuit and said transistor (311) have threshold values higher than that of the transistor having relatively low threshold value.

However, it would have been obvious for those skilled in the art to have changed the gate to source area of transistors of reference circuit to obtained desired threshold value(s), which can be either high/low depend on the intended use of the invention.

► With respect to claim 26, Tsuchi et al discloses a transistor (311) connected between said output terminal and said second power supply, having a threshold value higher than that of the transistor having relatively low threshold value and including a control terminal for receiving said control signal to be controlled to be on and off.

► With respect to claim 27, Tsuchi et al discloses the conductivity type of said output stage transistor (311) is opposite that of said differential pair (213,214).

► With respect to claim 29, Tsuchi (fig. 8, cols 1-44) discloses a differential amplifier circuit comprising:

- first and second input terminals (1, 2: for inputting signals to gates of transistors 213, 214, 223 and 224);
- an output terminal (2: for outputting signals from output transistors 311 and 411);
- a first differential stage (21) including:

a first differential pair (213,214) for differentially receiving signal voltage supplied to said first and second input terminals;

a first load element pair (211,212) connected between an output pair of the first differential pair (connection between transistor 211 & 213 and connection between transistor 212 & 214) and a first power supply (V_{DD}), said first load element pair being comprised of a transistor pair, conductivity type of which is opposite that of a transistor pair composing said first differential pair; and

a first current source (215) connected between said first differential pair and a second power supply (V_{ss}) and supplying a current to said first differential pair;

- a second differential stage (22) including:

a second differential pair (223, 224) for differentially receiving signal voltage supplied to said first and second input terminals (1, 2), conductivity type of which is opposite that of a transistor pair composing said first differential pair;

a second load element pair (221, 222) connected between an output pair of the second differential pair (connection between transistor 221 & 223 and connection between transistor 222 & 224) and said second power supply (V_{ss}), said second load element pair being comprised of a transistor pair, conductivity

type of which is opposite that of a transistor pair composing said second differential pair; and

a second current source (225) connected between said second differential pair (223, 224) and said first power supply (V_{DD}) and supplying a current to said second differential pair;

- a first output amplification stage (30) receiving an output of said first differential pair and outputting an output signal from said output terminal;
- a second output amplification stage (40) receiving an output of said second differential pair and outputting an output signal from said output terminal;

said first differential pair and/or said first load element pair being comprised of transistors each having relatively low threshold value;

said second differential pair and/or said second load element pair being comprised of transistors each having relatively low threshold value;

a first switch circuit (521/215) for controlling an activation and deactivation of said first differential stage, wherein said first switch circuit inherently includes a transistor (521) connected in series with said first current source (215) between said first differential pair (213,214) and said second power supply (V_{SS}), including a control terminal for receiving a first control signal for being controlled to be on and off, and

a second switch circuit (522/215) for controlling an activation and deactivation of said second differential stage, wherein said second switch circuit inherently includes a transistor (522) connected in series with said second current source (225) between said

second differential pair (223, 224) and said first power supply (V_{DD}), including a control terminal for receiving a second control signal for being controlled to be on and off.

Tsuchi et al does not expressly disclose in written disclosure that the transistors of said first and second switch circuits have threshold values higher than that of the transistor having relatively low threshold value.

However, it would have been obvious for those skilled in the art to have changed the gate to source area of transistors of reference circuit to obtained desired threshold value(s), which can be either high/low depend on the intended use of the invention.

► With respect to claim 30, Tsuchi (fig 8, col 1-44) discloses said first output amplification stage (30) includes a first output stage transistor (311) having relatively low threshold value connected between said output terminal and said first power supply; said second output amplification stage (40) includes a second output stage transistor (411) having a relatively low threshold value, connected between said output terminal and said second power supply; a third switch circuit (531) for controlling activation and deactivation of said first output amplification stage (30), including a transistor (531) connected in series with said first output stage transistor (311) between said output terminal and said first power supply, having a control terminal for a receiving said first control signal for being controlled to be on and off in phase with on and off of said first switch circuit; a fourth switch circuit (541) for controlling activation and deactivation of said second output amplification stage (40), including a transistor (542) connected in series with said second output stage transistor (411) between said output terminal and said second power supply, having a control terminal for a receiving said second control

signal for being controlled to be on and off in phase with on and off of said second switch circuit.

Tsuchi et al does not expressly disclose in written disclosure that the transistors in said third and fourth switch circuits have threshold values higher than that of the transistor having relatively low threshold value.

However, it would have been obvious for those skilled in the art to have changed the gate to source area of transistors of reference circuit to obtained desired threshold value(s), which can be either high/low depend on the intended use of the invention.

► With respect to claim 31, Tsuchi (fig 8, col 1-44) discloses said first output amplification stage (30) includes a transistor (311) connected between said output terminal and said first power supply and having a control terminal for receiving a first control signal for being controlled to be on and off in phase with said first switch circuit; and wherein said second output amplification stage (40) includes a transistor (411) connected between said output terminal and said second power supply and having a control terminal for receiving a second control signal for being controlled to be on and off in phase with said second switch circuit.

Tsuchi et al does not expressly disclose in written disclosure that the transistors in said first and second output amplification stages have threshold values higher than that of the transistor having relatively low threshold value.

However, it would have been obvious for those skilled in the art to have changed the gate to source area of transistors of reference circuit to obtained desired threshold value(s), which can be either high/low depend on the intended use of the invention.

► With respect to claim 32, Tsuchi (fig 8) shows said wherein said first output stage transistor (311) is a transistor, conductivity of which is opposite that of said first differential pair; and said second output stage transistor (411) is a transistor, conductivity of which is opposite that of said second differential pair.

► With respect to claim 33, Tsuchi (fig 8, cols 1-44) discloses the differential amplifier circuit according to claim 29, further comprising a circuit (10) for controlling to charge and/or discharge said output terminal at a predetermined timing before the output signal is output from said output terminal.

► With respect to claim 34, Tsuchi (fig 8, cols 1-44) discloses said first output amplification stage includes a current source (321) and a transistor (532) having a control terminal for receiving said first control signal for being controlled to be on and off in phase with said first switch circuit, connected in series between said output terminal and said second power supply; and wherein said second output amplification stage (40) includes a current source (421) and a transistor (542) having a control terminal for receiving said second control signal for being controlled to be on and off in phase with said second switch circuit, connected in series between said output terminal and said first power supply.

Tsuchi et al does not expressly disclose in written disclosure that the transistors of said first and second output amplification stage have threshold values higher than that of the transistor having relatively low threshold value.

However, it would have been obvious for those skilled in the art to have changed the gate to source area of transistors of reference circuit to obtained desired threshold value(s), which can be either high/low depend on the intended use of the invention.

► With respect to claims 36-37, Tsuchi (fig 8, col 1-44) discloses a differential amplifier circuit comprising:

a differential pair (213,214) for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair (211,212) connected between an output pair of the differential pair and a power supply, said load element pair comprises a pair of transistors having control terminal coupled; and

a current source (215) for supplying a current to said differential pair;

said differential pair and/or said load element pair being comprised of transistors each having relatively low threshold value;

said differential amplifier circuit further comprising a switch circuit (531,532) for controlling activation and deactivation, wherein switch circuit includes at least one transistor (531,532) including a control terminal for receiving a control signal to be controlled to be on and off, said switch circuit comprises a first switch (531) comprised of a transistor connected between said power supply and said coupled control terminals of said load element pair, and a second switch (532) comprised of a transistor having a connected between an output end of one transistor of said load element pair and said coupled control terminals; and wherein said first and second switches are controlled in

common to be on and off by a control signal supplied to control terminals of said transistors constituting said first and second switches.

Tsuchi et al does not expressly disclose in written disclosure that the transistors of said switch circuit have threshold values higher than that of the transistor having relatively low threshold value.

However, it would have been obvious for those skilled in the art to have changed the gate to source area of transistors of reference circuit to obtained desired threshold value(s), which can be either high/low depend on the intended use of the invention.

► With respect to claim 46, claim 46 discloses only intended use of the invention wherein disclosure of Tsuchi et al can be used in a memory device.

6. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horie et al [US 6,054,876].

Horie et al (fig 2 col 1-18) discloses a differential amplifier circuit comprising:

a differential pair (49a,50a) for differentially receiving signal voltage supplied to a input pair thereof;

a load element pair (51a,52a) connected between an output pair of the differential pair (connection between transistors 51a,49a and connection between transistors 52a,50a) and a power supply (V_{DD}); and a current source (48a, col 6 lines 47-50) for supplying a current to said differential pair wherein said current source is comprised of a transistor including a control terminal for receiving a bias voltage as a control signal to be controlled to be on and off; said differential pair, and/or, said load element pair being comprised of transistors each having relatively low threshold value.

Horie et al does not expressly teach said transistor (48a) having a threshold value higher than that of the transistor having relatively low threshold value.

However, it would have been obvious for those skilled in the art to have changed the gate to source area of transistors of reference circuit to obtained desired threshold value(s), which can be either high/low depend on the intended use of the invention.

7. Claims 42-43, 48 and 50-62, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchi [US 6,567,327] or Horie et al [US 6,054,876] as applied to claims 21, 24-25, 29, 35-36 above, in further view of Arai et al [US 5,644,146].

Tsuchi and Horie et al substantially discloses the claimed differentially amplifier circuit but do not expressly mention a use of TFT's including a polycrystalline silicon film as an active layer on an insulating substrate for each of transistors in the differentially amplifier circuit.

However, using TFT including a polycrystalline silicon film as an active layer on an insulating substrate for each of transistors in the differentially amplifier circuit has been known in the art. See Arai et al as an evidence that shows usingTFT including a polycrystalline silicon film as an active layer on an insulating substrate for each of transistors in the differentially amplifier circuit to provide a good yield rate production and excellent operation characteristic for differential amplifier circuit.

Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Arai et al, to use the thin film transistors as being claimed for the

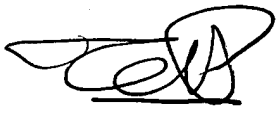
differentially amplifier circuit of Tsuchi or Arai et al to provide a good operation of the amplifier circuit as being mentioned above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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